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# PARTIAL WAFER BONDING AND DICING

## Abstract

Disclosed is a method of manufacturing integrated circuit chips that partially joins an integrated circuit wafer to a supporting wafer at a limited number of joining points. Once joined, the integrated circuit wafer is chemically-mechanically polished to reduce the thickness of the integrated circuit wafer. Then, after reducing the thickness of the integrated circuit wafer, the invention performs conventional processing on the integrated circuit wafer to form devices and wiring in the integrated circuit wafer. Next, the invention cuts through the integrated circuit wafer and the supporting wafer to form chip sections. During this cutting process, the integrated circuit wafer separates from the supporting wafer in chip sections where the integrated circuit wafer is not joined to the supporting wafer by the joining points. Chip sections where the integrated circuit wafer remains joined to the supporting wafer are thicker than the chips sections where the integrated circuit wafer separates from the supporting wafer.